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A NEW APPROACH TO THE DESIGN OF HIGHLY EFFICIENT REGULATED DC-T--ETC(U)
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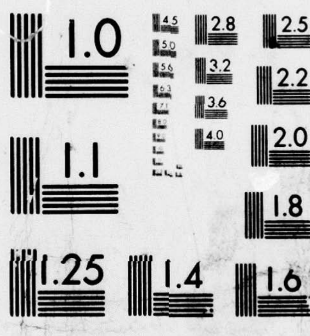

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This report describes a novel approach to the design of efficient switching regulated dc-to-dc converters whereby an energy storage inductor and a commutating diode are in the output transformer primary circuit of the converter. This design has advantages of simplicity, economy, and reliability in applications where high-output voltages, multiple-output voltages, or both are involved.

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FIGURES

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1. INTRODUCTION

Electronic power supplies are frequently required to perform the functions of (1) changing a single dc input voltage into one or more different output dc voltages and (2) regulating against changes in load or input voltage. In applications for which there is a large difference between input and output voltages or for which multiple output voltages are required, a dc-to-dc converter, with some means of regulation, is usually used. This application is the subject of this report.

Frequently, a dc-to-dc converter has been regulated by using a separate series-pass or switching regulator to regulate either the input or the output of the converter. A less costly and more efficient approach is to use the converter switching transistors to perform the function of a series-pass or switching regulator. The more efficient approach is the switching regulator mode. With the introduction of low-cost, integrated pulse-width-modulation (PWM) control circuits such as the Silicon General SG1524, the switching regulated converter has become economical as well as efficient.

A basic switching regulated converter circuit is shown in figure 1. When either transistor Q1 or transistor Q2 is conducting, the voltage at the input side of inductor L1 is at its maximum value. When neither Q1 nor Q2 is conducting, the voltage at the input side of L1 is at zero. The voltage at the output side of L1 is the time average of these two values. Hence, by controlling the ratio of on time to off time of Q1 and Q2, the output voltage can be regulated. L1 forms an integral part of the switching regulation system.

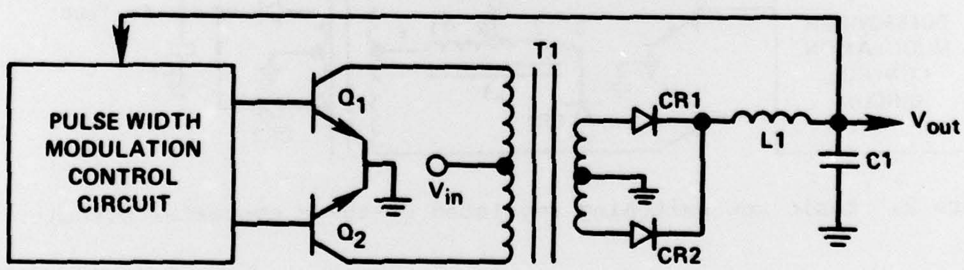


Figure 1. Basic switching regulated dc-to-dc converter circuit.

For many applications, the basic circuit of figure 1, or a similar circuit, is the optimum configuration. However, L1 can present a problem in two types of applications: (1) In applications requiring multiple output voltages, a separate inductor is required for each output. Using separate inductors increases component cost and the

printed circuit board area requirement. Also, multiple output voltages are difficult to regulate precisely. (2) In applications requiring high-voltage outputs, the required inductor consists of many turns of very fine wire and has low reliability and high cost. In addition, for high-frequency applications, the stray capacitance between turns grossly interferes with proper circuit operation. Another disadvantage is that, since voltage multiplier rectifier circuits cannot be used, a higher turns ratio is required for transistor T1. This ratio further degrades circuit reliability due to higher ac voltage and further degrades proper circuit operation due to higher stray capacitance in T1. Because of these problems, switching regulated converters have not generally been used in applications in which multiple outputs, high voltages, or both are required. This report describes a novel design for a switching regulated converter that overcomes these disadvantages by using a tapped inductor and a commutating diode in the primary circuit of T1 and eliminating the need for output circuit inductors.

2. BASIC DESIGN INFORMATION

One basic circuit configuration of the new switching regulated converter is shown in figure 2. This circuit is similar to that of figure 1 except for the addition of diode CR1 and tapped choke L1 and the substitution of a capacitor-input filter for the choke-input filter in the converter output circuit.

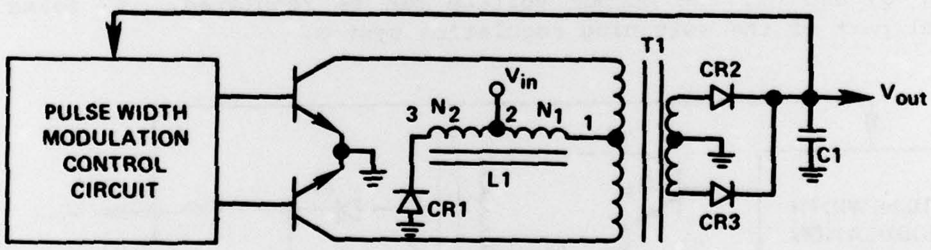


Figure 2. Basic new switching regulated dc-to-dc converter circuit.

In this circuit, the PWM control circuit is similar to that of figure 1, assuming that neither output transistor is operating at more than 50-percent duty cycle and that there is no time when both transistors are conducting at once. Thus, the effective converter input voltage (pin 1 of L1) is less than the input power voltage (V_{in}) during transistor live time. During transistor dead time, no current is drawn by either switching transistor and, hence, no current flows out of pin 1 of L1 into the output transformer. Since current flows during live time and the current through an inductor tends to continue flowing when the

circuit is interrupted, the voltage at pin 1 of L1 builds up to a value greater than the input voltage during dead time. When the voltage at pin 1 is increasing, the voltage at pin 3 is decreasing, until the voltage between pins 2 and 3 equals the input voltage, and commmutating diode CR1 begins to conduct. The current that had flowed through pins 2 and 1 of L1 into the converter becomes transformed by the ratio N_1/N_2 and flows through CR1. During converter live time, current flows out of the input supply and into the converter. During converter dead time, current flows through L1 (N_2) through CR1 and into the input supply. (In practice, the input supply is usually a capacitor isolated from the power source. This isolation is desirable because it assures that the energy flowing back into the power source is stored and not dissipated as heat.)

During converter live time, the instantaneous input voltage to the converter output transformer is less than the converter input voltage. This is the voltage that is stepped up or down by the transformer. Thus, the converter output voltage is proportional to this voltage. This portion of the circuit is redrawn in figure 3. For analyzing the voltage waveform at pin 1 of L1, this circuit is equivalent to that shown in figure 4. Important terms are defined as follows:

V ≡ input supply voltage.

V_x ≡ converter input voltage when one and only one switching transistor is conducting.

t_L ≡ transistor live time, time per cycle when one switching transistor is conducting.

t_D ≡ transistor dead time, time per cycle when that switching transistor is not conducting.

d ≡ transistor duty cycle = $t_L/(t_L + t_D)$.

During dead time the voltage at pin 1 of L1 is $[1 + (N_1/N_2)]V$. The average voltage across L1 must be zero so, during live time, the voltage at pin 1 must be $<V$. The following equation must be satisfied (assuming infinite inductance):

(voltage across L1 during dead time) (t_D) = (voltage across L1 during live time) (t_L)

or

$$\left(N_1/N_2\right)Vt_D = \left(V - V_x\right)\left(t_L\right) .$$

In terms of the transistor duty cycle,

$$\left(N_1/N_2\right)V(1 - 2d) = \left(V - V_x\right)(2d) \quad ,$$

$$V_x = V - \frac{VN_1(1 - 2d)}{2N_2d} \quad , \; d < 0.5 \quad ,$$

if $N_1 = N_2$, $V_x = 2V - V/2d$, $0.25 < d < 0.5$. Thus, V_x is inversely proportional to the duty cycle. As can be seen from this last equation, a 25-percent duty cycle gives $V_x = 0$ and, hence, zero converter output, whereas a 50-percent duty cycle gives $V_x = V$ for a 1:1 turns ratio. Thus, varying the duty cycle of the switching transistors varies the converter output voltage.

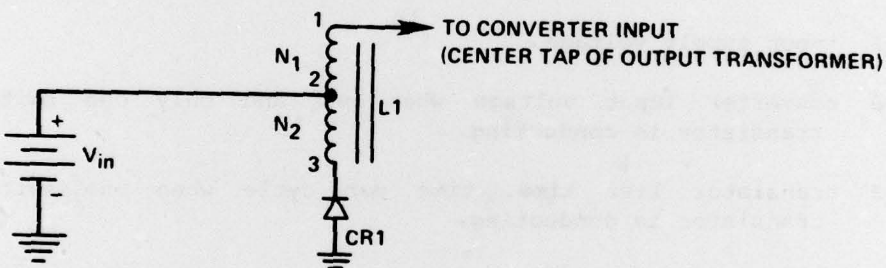


Figure 3. Circuit of inductor and commutating diode in switching regulated dc-to-dc converter circuit.

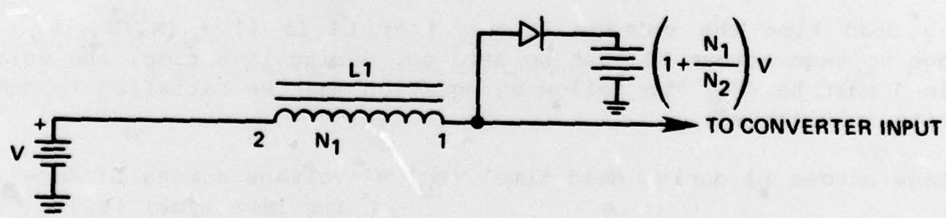


Figure 4. Equivalent circuit of inductor and commutating diode in switching regulated dc-to-dc converter circuit.

This discussion assumes that there is no time when both transistors are on simultaneously. If they are on simultaneously, pin 1 of L1 is effectively short-circuited to ground during this time. When only one transistor is conducting, the voltage at pin 1 is greater than the input voltage, that is, $V_x > V$. Thus, the mode of regulation differs if transistor overlap is allowed to occur. During this mode, CR1 does not conduct and, in some circuits, may be omitted along with winding 2-3 of L1.

The time when both transistors are conducting simultaneously is 2d - 1, whereas the time when only one transistor is conducting is 2 - 2d. For 0 Vdc across L1,

$$(V - 0)(2d - 1) = \left(V_x - V\right)(2 - 2d) \quad ,$$

$$V_x = V\left(\frac{1}{2 - 2d}\right) \text{ , } 0.5 \leq d < 1.0 \quad .$$

Thus, at zero overlap time and zero dead time (that is, 50-percent transistor duty cycle), $V_x = V$. As overlap time approaches 100 percent, V_x and, hence, converter output voltage approach infinity. For practical reasons, d must be limited to considerably less than 100 percent. The presence of CR1 and its associated winding on L1, if used, limits V_x to $(1 + N_1/N_2)V$, as is apparent from figure 4. However, it can be seen from the two equations for $d \leq 50$ percent and $d \geq 50$ percent that there is no discontinuity in the curve of d versus V_x. Thus, a regulator may be designed to operate through this point of d = 50 percent to give an extremely wide range of input voltage for regulation. Figure 5 shows a curve of V_x/V versus d for $N_1 = N_2$.

Although the design of the actual circuitry of a switching regulated dc-to-dc converter is assumed known by the reader, one peculiarity of this circuit that affects regulator loop design should be mentioned. In the circuit of figure 1, current through L1 always flows into the load. In regulator loop analysis, L1 and output capacitor C1 behave as a simple L-C filter with a 180-deg phase shift at higher frequencies. However, in the circuit of figure 2, when the switching transistor duty cycle is varied, not only does the current through L1 change, but the percentage of time that this current is allowed to flow into the load changes too. (The load represents C1 and the actual load reflected to pin 1 of L1 by the turns ratio of T1.) Thus, at high frequencies, the phase shift between a control voltage that is proportional to the duty cycle and the output voltage is only 135 deg--halfway between a pure capacitor (90 deg) and an L-C (180 deg). This phase shift has been verified experimentally.

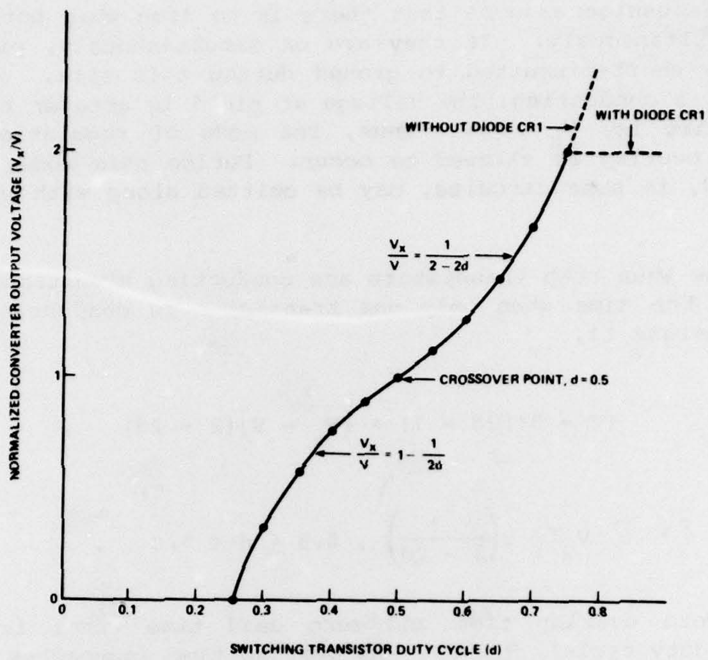


Figure 5. Normalized converter output voltage versus switching transistor duty cycle calculated for $N_1 = N_2$.

3. 30-W HIGH-VOLTAGE CONVERTER CIRCUIT

The 30-W high-voltage converter circuit (fig. 6), designed for a missile application, operates at 25 V ± 10 percent and produces +950 V at 32 mA. The output remains within ±1 V over the entire input voltage range, and rejection of low-frequency ripple superimposed on the input battery line is at least 39 dB over frequencies from 0 to 80 kHz. Efficiency is nominally 82 percent.

The pulse width modulator is made of U1 and associated circuitry. The 2.61-kΩ resistor and the frequency select resistor, together with the 0.002-μF capacitor, determine the operating frequency of the converter, 80 kHz. Pin 3 of U1 is used, with appropriate buffering, as an output at twice the converter frequency to synchronize other circuits.

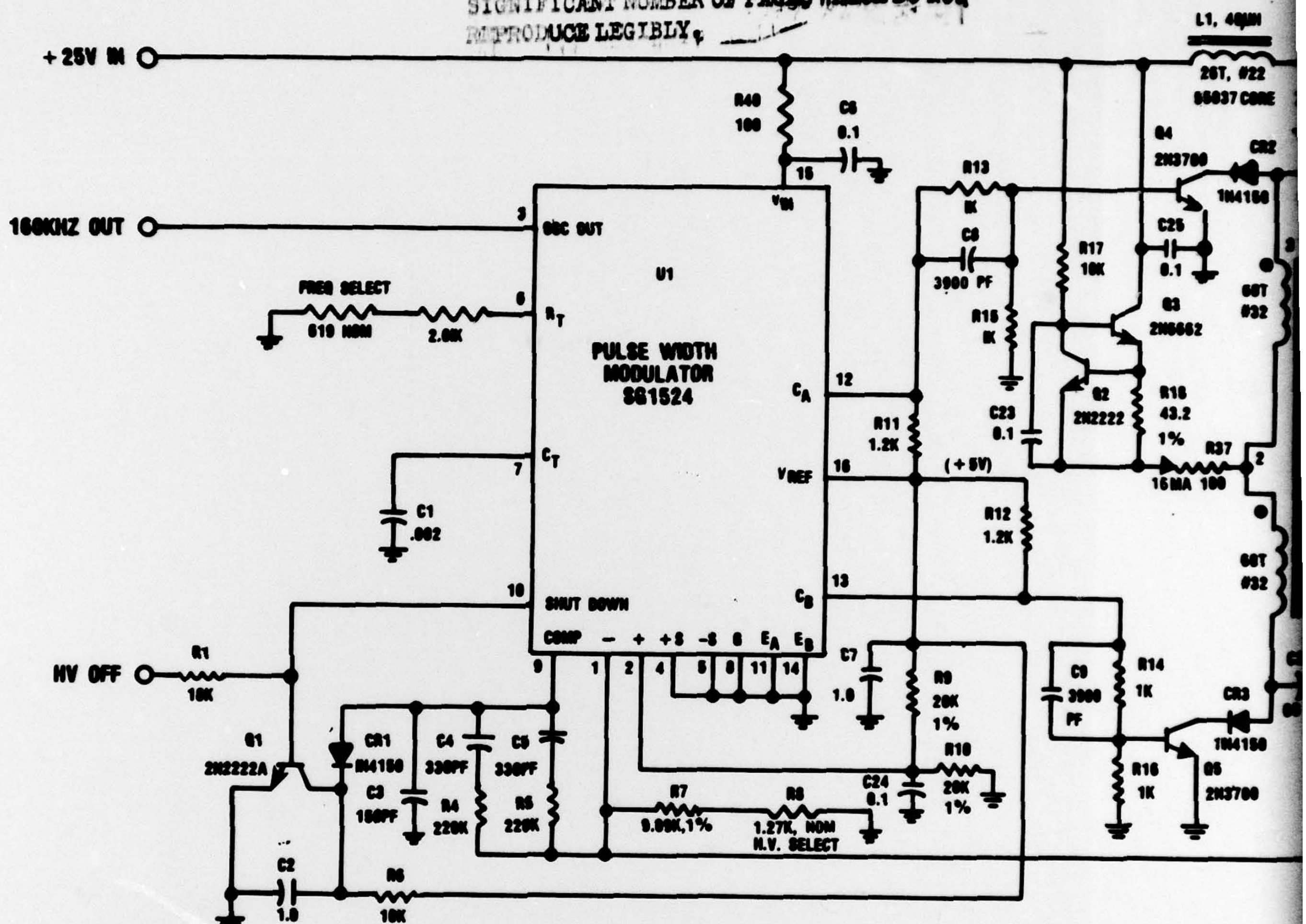
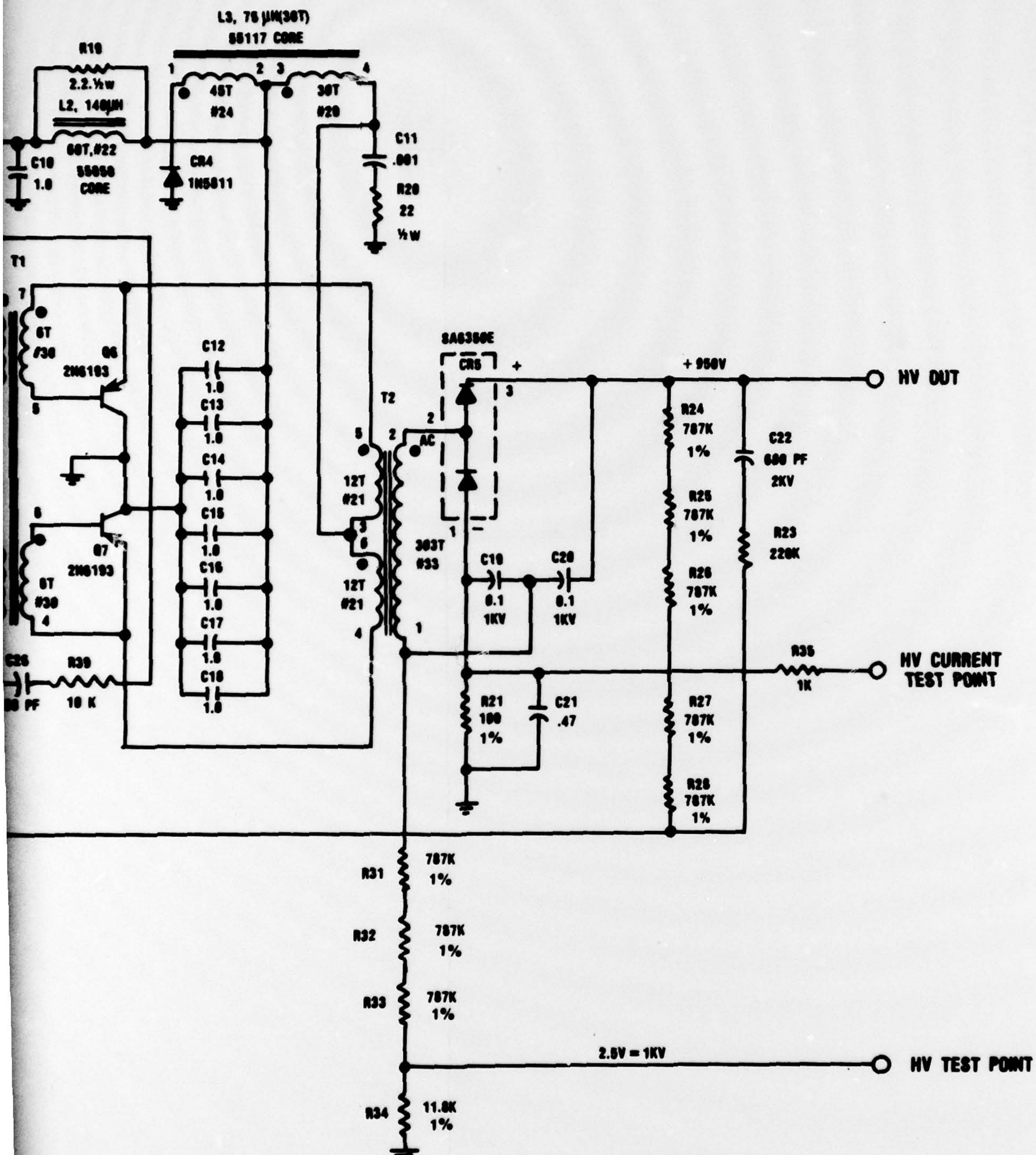


Figure 6. High-voltage converter



L3, 75 µH(30T)
55117 CORE
R19
2.2.½W
L2, 140µH
60T,#22
55050
CORE
45T
#24
30T
#20
C10
1.0
CR4
1N5811
C11
.001
R20
22
½W
T1
6T
#30
Q6
2N6193
Q7
2N6193
C12
1.0
C13
1.0
C14
1.0
C15
1.0
C16
1.0
C17
1.0
C18
1.0
R39
10 K
T2
12T
#21
303T
#33
SA6350E
CR5
AC
+ 950V
HV OUT
R24
787K
1%
R25
787K
1%
R26
787K
1%
C22
680 PF
2KV
R23
220K
C19
0.1
1KV
C20
0.1
1KV
R21
100
1%
C21
.47
R35
1K
HV CURRENT
TEST POINT
R27
787K
1%
R28
787K
1%
R31
787K
1%
R32
787K
1%
R33
787K
1%
2.5V = 1KV
HV TEST POINT
R34
11.8K
1%

r circuit.

2

The collectors of the two output transistors of U1 are brought out at pins 12 and 13. These transistors operate at less than a 50-percent duty cycle with no overlap. These outputs, in turn, drive driver transistors Q4 and Q5 through resistors R13 to R16 with speedup capacitors C8 and C9. R11 and R12 supply collector voltage to the SG1524 output transistors. Q4 and Q5, being used in an inverting configuration, operate at greater than a 50-percent duty cycle, and thus overlap occurs when they are both on the same time. The driver circuit consists of Q4 and Q5, diodes CR2 and CR3, the current source, and driver transformer T1. When only Q4 or Q5 is on, current from the current source (16 mA) is stepped up by the turns ratio of T1 to drive Q6 or Q7. When both Q4 and Q5 are on, there is an effective short circuit across T1, thereby removing base drive from both Q6 and Q7. CR2 and CR3 prevent reverse collector-emitter voltage across Q4 and Q5 during switching. The current source, consisting of Q2, Q3, R17, R37, and C23, supplies approximately 16 mA to the base drive transformer at room temperature. C23 is a bypass, which insures good high-frequency response of the current source while R37 suppresses parasitic oscillation. The damping network consisting of R39 and C26 suppresses high-frequency spikes in the driver circuit that had caused regulator loop instability in an earlier design without these components.

Due to high ripple current present at the center tap of the primary coil of T2, it was necessary to parallel several 1-μF ceramic capacitors to obtain sufficient capacitance and to reduce ripple current in each one. (Due to a high equivalent series resistance (ESR) and low ripple current ratings, solid tantalum capacitors would have been a poor choice.) A turns ratio of 1.5:1, rather than 1:1, was chosen for L3 because this ratio experimentally produced greater converter efficiency and reduced voltage stress on Q6 and Q7. C11 and R20 form a despiking network. The battery input filter consists of L1, C10, L2, R19, and C12 through C18. R19 is a damping resistor to improve ripple rejection response and prevent parasitic oscillation. Due to the low value of R19, it was necessary to add L1 and C10 to improve high-frequency ripple rejection characteristics.

The secondary coil of T2 drives a full-wave voltage doubler consisting of CR5, C19, and C20. A current sensing resistor, R21, in series with the negative output of the high-voltage rectifier circuit, bypassed by C21, senses the high-voltage output current. This test point is isolated by R35.

The high voltage is monitored by dividing down half of the voltage doubler output to approximately 2.5 V by R31 to R34. For regulation, the entire high-voltage output is divided down to approximately 2.5 V by R24 to R28, R7, and select resistor R8. Several resistors were used in series for the high-voltage application because of voltage derating criteria. For economy, the high-voltage test point was taken from the

voltage divider center tap. However, due to the higher amplitude and the lower frequency of ripple appearing at this tap, this point was not suitable for regulator feedback. C22 and R23 form a phase lead compensation network for optimum regulator loop performance. Phase lag compensation is achieved by C3, C4, C5, R4, and R5. Redundancy for C4-R4 and C5-R5 insures that if one of these components fails, the regulator loop will remain stable. An unstable, but otherwise operable, power supply will cause severe problems in this application.

R9 and R10 divide down the U1's internal 5-V reference to 2.5 V for use as a reference voltage. C6, C7, and C24 are high-frequency bypass capacitors.

C2, R6, and CR1 form a soft-start circuit that causes the output duty cycle to increase slowly from zero to the point of regulation when power is first applied or when the "HV OFF" input first goes low. This circuit prevents severe transients from momentarily overstressing the output transistors. Q1 discharges C2 and shuts off the high voltage when the "HV OFF" input is high. The "SHUT DOWN" input of U1 contains a shutdown circuit, which is used primarily as a 15-kΩ resistor from the base of Q1 to ground.

4. TEST RESULTS ON 30-W CONVERTER

Five converters were built and tested at room temperature, and one breadboard of the converter design was tested over the temperature range of -40 to +75 C. The results of these tests are shown in table 1 (p. 14). Typical converter switching waveforms are shown in figure 7 (p. 15). The unusual Q6 emitter waveform shows the four distinct sequential states of (1) Q6 on, (2) both transistors off, (3) Q7 on, and (4) both transistors off again. However, the waveform across the primary coil of output transformer T1 in figure 2 or T2 in figure 6 is approximately a square wave.

5. CONCLUSIONS AND RECOMMENDATIONS

The power supply design shown in figure 6 has proven to be successful and has met all its criteria. The efficiency of this power supply is over 80 percent, which is much higher than that of other designs typically used for high-voltage converters. This high efficiency has allowed the use of small TO-5 switching transistors, eliminated the need for a series-pass transistor, and considerably reduced space required and heat generated. Although extensive reliability data have not been gathered, none of the five configured converters that have been built have failed except that one U1 failed due to transients on the 25-V input caused by defective test equipment.

TABLE 1. REQUIREMENTS AND MEASURED DATA FOR HIGH-VOLTAGE CONVERTER

Parameter	Specification limit (at +25 C)	Breadboard -40 C	Breadboard +25 C	Breadboard +75 C	Brassboard C (5 units, +25 C) Mean	Brassboard C (5 units, +25 C) Range
High voltage out	950 ± 4 V	943 V	951 V	957 V	949.8 V	948 to 952 V
High voltage out for V_{in} ± 5%	0 ± 1 V	--	--	--	0.002 V	0 to 0.1 V
Input current R_L = 30.3 kΩ	1.6 A max	1.39 A	1.42 A	1.47 A	1.45 A	1.44 to 1.46 A
High-voltage ripple	1.0 V rms max	--	--	--	0.27 V	0.24 to 0.29 V
Input ripple	70 mV rms max	--	--	--	12.3 mV	10.8 to 14.6 mV
Efficiency	80% min	84%	84%	82%	81.4%	80.2 to 82.2%
Ripple rejection ratio*						
1 kHz	--	-49 dB	-49 dB	-46 dB	-48 dB	-46 to -51 dB
4 kHz	--	-40 dB	-39 dB	-39 dB	-42 dB	-41 to -44 dB
10 kHz	--	-48 dB	-48 dB	-46 dB	-48 dB	-46 to -50 dB

$$*\text{Ripple rejection ratio} = \frac{\dfrac{\text{ac ripple out}}{\text{dc } V_{out}}}{\dfrac{\text{ac ripple in}}{\text{dc } V_{in}}}$$

Rejection of low-frequency ac input ripple superimposed on the 25-V input line was very good with this circuit, although a series-pass regulator would have been superior at the expense of efficiency. Most series-pass regulators do not need fast loop response to reject changes in input voltage. However, in switching regulators, the operating duty cycle must change in response to the changes in input voltage, which requires fast regulator loop response. In the circuit of figure 6, low-frequency ripple (below 4 kHz) is rejected mostly by fast regulator loop response, and high-frequency ripple (above 4 kHz) is rejected mostly by passive filtering from L1, C10, L2, and C12 to C20 (fig. 6). Ripple rejection is limited by regulator loop stability considerations and passive component bulk restrictions. However, the ripple rejection is adequate for the intended application, and many applications do not have ripple rejection requirements.

(a)

(b)

(c)

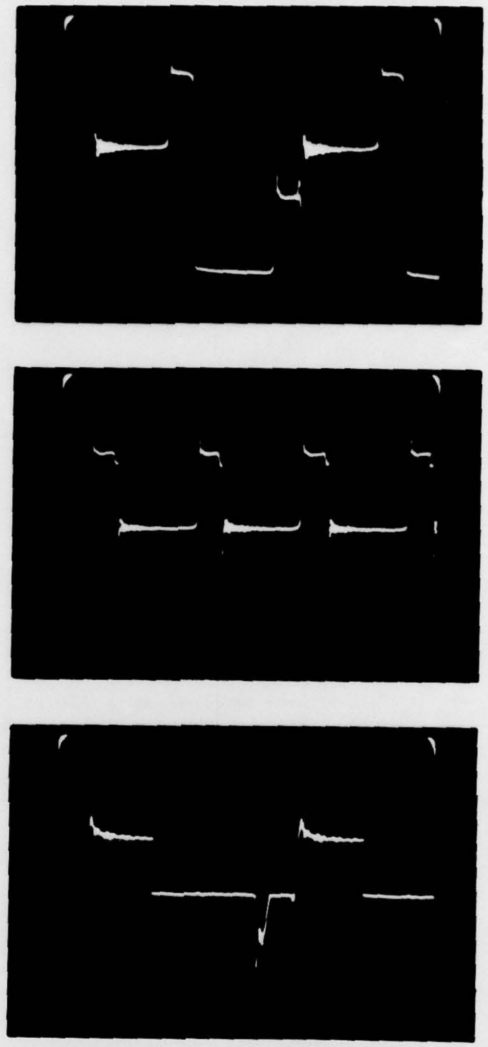


Figure 7. Typical high-voltage converter switching waveforms at (a) transistor Q6 emitter, (b) pin 4 of inductor L3, and (c) pin 1 of transformer T1 (ordinate units are 10 V/div; abscissa units are 2 μs/div).

It is recommended that the use of the basic new switching regulated dc-to-dc converter circuit (fig. 2) be considered for regulated dc-to-dc converter applications requiring either multiple output voltages or high-voltage output. The advantages will be simplicity and efficiency; reductions in size, power consumption, heat production, and cost; and a potential improvement in reliability.

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